Notice of Allowability	Application No.	Applicant(s)	
	09/966,588	SAWEY ET AL.	
	Examiner	Art Unit	
	Thai D. Hoang	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed on 09/28/2001*.

2. ☒ The allowed claim(s) is/are *1, 4-32 have been renumbered as 1-30 respectively*.

3. ☒ The drawings filed on *23 January 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jessica Smith on June 9, 2005.

The application has been amended as follows:

Claim 1: (Currently Amended) A system for processing digital signals, comprising:

a pointer follower to receive a first digital signal having a first signal frame, first embedded payload and a pointer follower ("PF") pointer, extract said first embedded payload from said first digital signal and forward said first embedded payload;

an elastic buffer in electrical connection with said pointer follower operable to receive, delay and forward said first embedded payload;

a pointer generator to receive said first embedded payload and a synchronization pulse and construct a new digital signal comprising said first embedded payload, a new signal frame, and a pointer generator ("PG") pointer, wherein the location of said new signal frame within said new digital signal determined according to said synchronization pulse; and

a synchronization module to generate said synchronization pulse according to a predetermined schedule and communicate said synchronization pulse to said pointer generator[[.]];

a first comparator operable to compare the value of said PF pointer and the value of said PG pointer and generate a pointer offset signal; and

a second comparator operable compare said pointer offset signal a target offset signal, generate an increment/decrement request signal based on the comparison, and communicate the increment/decrement request signal to said elastic buffer; and

wherein said elastic buffer delays said embedded payload according to said increment/decrement signal;

a PG counter synchronized according to said synchronization pulse;

a PF counter to track the location of said signal frame of said first digital signal; and

a third comparator to measure the offset between said PG counter and said PF counter.

Claims 2 and 3: have been canceled.

Claim 4: line 1, the statement "Claim 3" has been changed to – Claim 1--

Allowable Subject Matter

Claims 1, 4-32 have been renumbered as 1-30 respectively.

Claims 1-30 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Chaudhuri et al, US Patent No. 5,051,979, discloses a method and apparatus for errorless switching. Chaudhuri does not teach or fairly suggest the following features, which are recited in each independent claim of the present application:

(a) A system for processing digital signals, comprising:

a pointer generator (PG) counter synchronized according to said synchronization pulse;

a pointer follower (PF) counter to track the location of said signal frame of said first digital signal; and

a third comparator to measure the offset between said PG counter and said PF counter as recited in independent claim 1.

(b) A system for processing digital signals, comprising:

a first adder circuit and a second adder circuit, wherein the second adder circuit comprises:

a second pointer generator to receive a second embedded payload and construct a second new digital signal comprising the second embedded payload, a second new signal frame and a second PG pointer, wherein the location of the second new signal frame within the second new digital signal is determined by a synchronization pulse and wherein said second new signal frame is aligned with a first new signal frame of the first adder circuit as recited in independent claims 5 and 17.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited to further show the state of the art with respect to the application:

US Patent No. 5,631,896 A, Kawase et al., "Hitless path switching apparatus and method."

US Patent No. 6,246,668 B1, Kusyk, "Hitless manual path switching using linked pointer processors."

The following publications are cited to further show the state of the art with respect to the application:

Acharya, S.; Gupta, B.; Risbood, P.; Srivastava, A.; *"Hitless network engineering of SONET rings"*; Global Telecommunications Conference, 2003. GLOBECOM '03. IEEE Volume 5, Page(s): 2735 – 2739; 1-5 Dec. 2003.

Shrikhande, K.; Ikoma, Y.; Nakamura, A.; Kyeong Soo Kim; Horie, K.; Kazovky, L.G.; *"Hitless wavelength add-drop using a novel signaling protocol combined with hitless switching techniques"*; Optical Fiber Communication Conference and Exhibit, 2002. OFC 17-22 March 2002 Page(s): 740 – 742.

Ohta, H.; Ueda, H.; *"Hitless line protection method for ATM networks"*; Communications, 1993. ICC 93. Geneva. Technical Program, Conference Record, IEEE International Conference on 23-26 May 1993; Vol.1, Page(s): 272 – 276.

Iselt, A.; *"A new synchronization algorithm for hitless protection switching in ATM networks"*; Performance, Computing and Communications Conference, 1999. IPCCC '99. IEEE International 10-12 Feb. 1999 Page(s): 370 – 376.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai D. Hoang whose telephone number is (571) 272-3184. The examiner can normally be reached on Monday-Friday 10:00am-18:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Hoang

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

6/10/05